

IN THE DRAWINGS:

Attached are replacement sheets of drawings for Figs. 4 and 6.

REMARKS

Claims 1 - 30 are in the application and are presented for consideration. By this Amendment, Applicant has made clarifying changes to some of the claims including the independent claims 1 and 15. Favorable consideration of the claims as now presented is requested.

Claims 4 and 15 - 22 have been objected to based on informalities. Applicant has made changes to address these issues.

The drawings have been objected to because reference numerals 22 and 13 are not present in the drawings. These have now been added with the attached replacement sheets which add numerals 22 and 13 to Figs. 4 and 6 respectively. Approval of these changes is requested.

The specification has been objected to based on informalities. Applicant has amended the text with replacement paragraphs to address the issues raised.

Claims 1 - 30 have been rejected as being indefinite. The claims have been revised paying close attention to the Examiner's comments. Applicant wishes to thank the Examiner for the careful reading of the claims and for the helpful comments. It is believed that the claims as now presented are clear and definite and conform with the requirements of the statute.

Claims 1 - 4, 6 - 8 and 10 - 14 have been rejected as being obvious based on Kolchinsky in view of Schwenke et al. Apparatus claims 15 - 20 and 24 - 30 have been rejected based on Kolchinsky in view of Schwenke et al. The rejections are each based on the position that

Kolchinsky uses historical process data used by a programmable logic control and particularly wherein the historical process data are fed to the PLC to provide a virtual processing. The secondary reference Schwenke et al. is cited for disclosing a system with process data generated. The rejection takes the position that it would be obvious to use the virtual processing taught by Kolchinsky in the actual process or arrangement of Schwenke et al.

Kolchinsky (US 5,535,406) relates to a virtual processor module with a programmable matrix for improving the internal processing of data in a computer. Kolchinsky teaches dividing complex computation functions into a plurality of simple partial functions. These simpler functions are stored temporarily, in order to process them separately and to merge them again later. Consequently, this pertains to a time-effective running of computation operations within a computer hardware. Essentially this has nothing to do with the control of industrial processes per se. Therefore, production processes of an industrial plant are not mentioned in Kolchinsky.

Kolchinsky is essentially non-analogous prior art. Specifically, Kolchinsky presents teachings addressing issues as to using application specific computers and the difficulty of doing this in the past. Kolchinsky is based on the use of field programmable gate arrays (FPGA) allowing logic circuits for a machine to be configured allowing a special processor for a particular application to be provided. According to Kolchinsky a reconfigurable programmable logic device (such as an FPGA) is used for processing complex applications. This processor (referred to as virtual processor module) divides complex operations into a series of simpler operations with these being optimized. A programmable logic device is dynamically modified by a processor to be compatible with the rest of the system. As such, Kolchinsky does not

suggest features according to the invention. Instead, Kolchinsky relates to the internal operations of the processor and may be considered non-analogous prior art in the present application.

Schwenke et al. (US 6,556,950) is analogous prior art. Schwenke et al. does pertain to production processes in an industrial plant. Even though Schwenke et al. also describes a PLC memory (mapping table), in which input and output data per se are stored, which can then be used additionally for a simulation process, these input and output data (I/O data) do not originate from an earlier production process. Instead Schwenke et al. teaches generating data artificially, during the configuration of the simulation environment. As such, the prior art fails to suggest the combination of features claimed. The prior art does not suggest using historical process data from an actual earlier process run-through and processing such historical process data by the PLC or another PLC program logic in the same way as actual current process data.

Accordingly, Schwenke et al. represents the closest analogous prior art. However, Schwenke et al. fails to suggest the invention. The pertinent prior art as a whole fails to suggest the combination of features claimed. The claimed method and apparatus improve on the Schwenke et al. type system. As noted Kolchinsky pertains only to internal operations in a processor. This is non analogous and fails to provide a suggestion as to modifying the teachings of the related analogous art.

The person of ordinary skill in the art in the field that is relevant here and in the field of Schwenke et al. (US 6,556,940), namely the field of industrial plant controls is a person skilled in the art in the area of such controls. By contrast, the person skilled in the art of the

Kolchinsky (US 5,535,406) reference is skilled in computation particularly, namely computer processing per se. These are non analogous arts and the solutions and concepts of processing do not cross over to process control. Problems and attributes of such process control and related considerations are different and unique as compared to processing optimization. When a person skilled in the art considers improving such a control in the art according to Schwenke et al (US 6,556,950), the person skilled in the art in the area of industrial plant controls, especially PLCs, will not look to processing optimization or optimizing the internal control of computers, more specifically processors, as this happens in the subject of Kolchinsky (US 5,535,406), in order to find suggestions for improving a PLC industrial plant control. Even with knowledge of Kolchinsky, the person of ordinary skill in the industrial plant controls field will not look to Kolchinsky for solutions or ideas. Kolchinsky presents a completely different subject and deals with problems that are essentially different and which do not carry over to solve the problems faced in the industrial plant control field.

Schwenke et al. indisputably does not pertain to the use of historic process data obtained from a real run in a machine. Applicant's claims highlight the important aspect of the invention wherein historical data is used. Historical data is clarified as actual earlier process run-throughs, namely actual prior process data. Such actual process data is fed to the PLC or another PLC program logic in the same way as if the data came directly from the plant periphery, namely the actuator sensors etc. As such the historical process data is used as if it is current process data. This is clearly neither taught nor suggested by the prior art as a whole.

The underlying idea of the solution according to the present invention, namely, to use

such historic process data obtained in a real process to control the plant in view of the goals mentioned in the specification, especially on page 2, is therefore not contained in the above-mentioned document and it indisputably also fails to provide the person skilled in the art with any corresponding suggestions.

The rejection is based on the position that Kolchinsky discloses that historic process data are stored in a PLC in the form of a virtual processor, for which he refers to the abstract of the document.

The claims highlight more clearly, the use of historic process data in the sense of the present invention, namely data that are obtained in an earlier production process of the plant and are stored and are again sent to the control in order to reproduce this process. The generation of such data is not disclosed in Kolchinsky (US 5,535,406) and is not addressed there in any way.

Kolchinsky is focused toward a virtual processor with a reconfigurable programmable logic matrix for treating data per se in agreement with a hardware-coded algorithm. Furthermore, a memory is provided for storing a plurality of hardware configuration files for the programmable logic matrix, each configuration file being used to program an algorithm. The logic matrix has, furthermore, the matrix array inputs and outputs for data per se. Furthermore, a VPN controller for controlling the operation of the virtual processor with the functions described in the abstract as well as a data bus controller for controlling the data flow and a configuration controller are provided.

Data are processed per se with the subject of Kolchinsky, as it is done by any computer

or processor. Input data, which will be processed, and output data, which are the result of the processing, are mentioned in this connection, as this is also common in any computer.

In respect to the data, Kolchinsky does not consequently offer the person skilled in the art anything more than what is already known to him from any computer or processor per se. It is not stated anywhere in the document that the data obtained during the operation of a technological plant are historic data and that such may be used as claimed. Kolchinsky represents non-analogous solutions to non-analogous problems. Kolchinsky does not disclose to the person of ordinary skill in the art any more than what is already known to such person from any computer or processor anyway.

On the whole, it can therefore be stated that Kolchinsky (US 5,535,406) also fails to be able to provide the person of ordinary skill in the art with any suggestion on how to address problems in the field of the Schwenke et al. reference or to improve upon this system in the sense of the present invention, especially in the form of the newly presented claim. Even with knowledge of Kolchinsky, Kolchinsky only suggests how to divide complex internal computation tasks of the computer among a plurality of simple partial computation tasks within the computer. The fact that parts of the computation tasks and/or results are stored temporarily has nothing to do with data of such an industrial process, which are recorded in real industrial plants, i.e., with historic process data. In this sense, Kolchinsky (US 5,535,406) also fails to make any statement about additionally entering any data, let alone industrial process data, into a PLC. Kolchinsky does not deal with such issues whatsoever.

In summary, Applicant requests consideration of the following points:

Schwenke et al. is analogous prior art (which pertains to the control of industrial plants).

Kolchinsky is non-analogous prior art (and pertains to the internal operation of the processing of computing functions in a processor).

The person of ordinary skill in the art of the invention is concerned with developing and improving systems as disclosed by Schwenke et al. and is not specifically concerned with the internal operation and optimization of the processing of computing functions in a processor.

Kolchinsky addresses a pure computer expert rather than the person skilled in the art of industrial plant controls, and the person skilled in the art of industrial plant controls does not look to such teachings for developing and improving systems as disclosed by Schwenke et al.

Kolchinsky fails to offer the person skilled in the art in the field of industrial plants any suggestions for developing and improving the subject of US 6,556,950. There are no suggestions to provide the combination according to the present invention.

Claims 5 and 9 have been rejected as being obvious based on Kolchinsky in view of Schwenke et al. and further in view of Burshtein et al. Although Burshtein et al. teaches the use of time markers, the references as a whole fail to suggest the combination of features claimed. The references do not suggest the invention and therefore all claims define over the prior art as a whole.

Applicant respectfully requests that the Examiner favorably consider the claims as now presented in view of the changes made to the claims and in view of the discussion above. Should the Examiner determine that any issues remain which have not been resolved, the Examiner is requested to telephone Applicant's attorney such that all issues may be resolved

at an early time.

Respectfully submitted
for Applicant,



By: _____
John James McGlew
Registration No. 31,903
McGLEW AND TUTTLE, P.C.

JJM:jj/tf
71066-6

Attached: (2) Replacement Sheets of Drawings

DATED: June 26, 2006
BOX 9227 SCARBOROUGH STATION
SCARBOROUGH, NEW YORK 10510-9227
(914) 941-5600

SHOULD ANY OTHER FEE BE REQUIRED, THE PATENT AND TRADEMARK OFFICE
IS HEREBY REQUESTED TO CHARGE SUCH FEE TO OUR DEPOSIT ACCOUNT 13-
0410.